**Objection to Fig. 3**

Regarding the Examiner's objection to Fig. 3, Applicants propose amending Fig. 3 to include the legend --Prior Art--, as shown in the accompanying Request for Approval of Drawing Change. Accordingly, the objection to Fig. 3 should be withdrawn.

**Objection to the Drawings under 37 CFR § 1.83(a)**

Regarding the Examiner's objection to the drawings for failing to show input/output cells as recited in claim 1, Applicants have canceled this feature from the claim.

Regarding the Examiner's objection to the drawings for failing to show first and second I/O slots arranged on the same wiring layer, Applicants amend the term "wiring layer" in claim 1 to "wiring level." Fig. 2, for example, shows first and second I/O slots arranged on the same wiring level.

Regarding the Examiner's objection to the drawings for failing to show a first pad arranged on a wiring layer different from said first I/O slot, and a second pad arranged on a wiring layer different from the first I/O slot, Applicants amend the term "wiring layer" in claim 1 to "wiring level." Fig. 2, for example, shows a first pad arranged on a wiring level different from said first I/O slot, and a second pad arranged on a wiring level different from the first I/O slot.

Accordingly, the objection to the drawings under 37 C.F.R. § 1.83(a) should be withdrawn.

Regarding the objection to the drawings for the alleged inconsistency between Figs. 1 and 2, Applicants propose amending Fig. 2 to show four broken lines connecting via 15 and via 35 and four broken lines connecting via 18 and via 25 and to correct lines

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

of vias 15, 35, 18, 25 and 23 from solid to dashed or vice versa, as shown in the accompanying Request for Approval of Drawing Change. Accordingly, the objection to the drawings is deemed overcome.

In making these references to the drawings, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation and applicable case law.

**Objection to the Specification under 35 U.S.C. § 132**

Regarding the § 132 objection to the specification, based on the allegation that new matter was introduced by Applicants' amendment filed on April 24, 2002, Applicants amend the term "wiring layer" in claim 1 to "wiring level." Fig. 2, for example, shows a first pad arranged on a wiring level different from said first I/O slot, and a second pad arranged on a wiring level different from the first I/O slot. (Also see pages 8 and 9 of the present application.) Accordingly, the objection to the specification under 35 U.S.C. § 132 should be withdrawn. Applicants also note

**Rejection under 35 U.S.C. § 112, first paragraph**

Similarly, regarding the rejection under 35 U.S.C. § 112, first paragraph of claims 1 and 4-14, based on an allegation that the claims contain subject matter which was not sufficiently disclosed in the specification, Applicants amend the term "wiring layer" in claim 1 to "wiring level." Fig. 2, for example, shows a first pad arranged on a wiring level different from said first I/O slot, and a second pad arranged on a wiring level different from the first I/O slot. (Also see pages 8 and 9 of the present application.)

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Accordingly, the § 112, first paragraph rejection of claims 1 and 4-14 should be withdrawn.

**Rejection under 35 U.S.C. § 103(a)**

To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. §2143 (8th ed. 2001)).

Regarding the rejection under 35 U.S.C. §103(a) of claims 1 and 4-14, claim 1 recites first pad "arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot," and a second pad "arranged on a wiring level different from said first I/O slot and arranged apart from the peripheral portion of the chip as compared with the first pad."

In contrast, Applicants' so called admitted prior art (Fig. 4) discloses a first pad 12a arranged above a first I/O slot 11a and connected to the first I/O slot 11a. Thus, Applicants' so-called admitted prior art does not disclose or suggest at least a first pad "arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot," as recited in claim 1.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Janai discloses a customizable three metal layer gate array device. Janai fails to disclose or suggest at least a structure wherein a first pad is "arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot," as recited in claim 1. Because Janai does not cure the deficiencies of Applicants' so called admitted prior art, the § 103(a) rejection of claim 1 should be withdrawn. Further reasons supporting patentability of claim 1 are provided below.

Claim 1 also recites a third wiring "arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot." The Examiner admits at page 4 of the Office Action that "the admitted prior art does not disclose a third wiring." The Examiner characterizes vertical metal strips M2 of Janai as the claimed third wiring. However, Janai discloses that vertical metal strips M2 overlies the M1 layer (col. 2, line 58). As shown in Fig. 1A of Janai, vertical metal strips M2 are not "arranged in an outermost peripheral region of the chip," as recited in claim 1. Because a combination of Applicants' so called admitted prior art and Janai does not teach at least the claimed third wiring, the § 103(a) rejection of claim 1 should be withdrawn.

Further, the Examiner did not provide any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Even if such a combination were proper, a reasonable expectation of success would not exist.

The § 103(a) rejection of claims 6-8 and 10 should be withdrawn as well, at least in view of their dependence from allowable claim 1.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

New claims 15-20 are allowable as well, at least in view of their dependence from allowable claim 1.

## CONCLUSION

Attached hereto is a marked-up version of the changes made to the claims by this amendment. The attachment is captioned "**Appendix to the Amendment of October 10, 2002**" Deletions appear as normal text surrounded by [ ] and additions appear as underlined text.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 19, 2003

By: Tara Bleech
Tara L. Bleech
Reg. No. 46,559

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

**APPENDIX TO AMENDMENT OF FEBRUARY 19, 2003**

**Version with Markings to Show Changes Made**

Amendments to the Claims

Please amend claims 1 and 10, as follows:

1. (Amended Three Times) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged on the same wiring [layer] level in parallel along a peripheral portion of a chip within an inner region of the chip [and connected to input/output cells of the chip];

a first pad arranged on a wiring [layer] level different from said first I/O slot and arranged above the first I/O slot;

a second pad arranged on a wiring [layer] level different from said first I/O slot and [comprising a predetermined distance apart from the first pad in a direction extending] arranged apart from the peripheral portion of the chip [toward the central portion] as compared with the first pad;

a first wiring comprising one end positioned in said first pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring comprising one end positioned in the second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot; and

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

a third wiring arranged in an outermost peripheral [portion] region of the chip and serving to connect the other end of the first wiring to [the second I/O slot] an I/O slot different from the first I/O slot[; and

a fourth wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot].

10. (Twice Amended) The semiconductor integrated circuit device according to claim [9] 1, further comprising a fourth wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com